The Embedded Muse 61

FPGAs

EE Times magazine is a weekly newspaper-like publication that covers both business and technology news for electronic engineers.

The February 5, 2001 issue contains a short but interesting column by Ron Wilson where he ponders the question, "Have FPGAs taken the wrong road?" An intriguing query, indeed, and one I've thought about much in the last year or so.

ASICs get all of the press and glory now, with system-on-a-chip (SOC) technology sometimes sounding like the only way anyone can make a product. But building an ASIC is prohibitively expensive unless your volumes are huge. That's where FPGAs and PLDs traditionally come in, at lower volumes that do need high levels of integration.

This view of the FPGA as a poor man's ASIC is, in my opinion, flawed. Or at least narrow. Sure, it's nice to cram a bunch of logic into one big part, reducing PCB space, costs, and power dissipation.

But we forget that an FPGA is *programmable*. You don't have to use it for a fixed design.

The coolest example of this that I know of is the PodAlyzer, a very cheap logic analyzer introduced four or five years ago. I suspect it's not available anymore as their web site is gone. The unit acquires 18 digital channels at 100 MHz, yet is the size of a pocket knife. A serial cable runs from the unit to a PC which displays results and interacts with the user.

The secret to the PodAlyzer's small size is the use of a dynamically reconfigurable FPGA. It bypasses all of the complex logic needed for multi-level triggering by simply connecting all 18 inputs to a small FPGA. When you specify a trigger sequence, the PC-hosted software actually redesigns the FPGA to detect the sequence you want! Quickly, too – there's no noticeable delay. The new design is sent down the serial link and the unit monitors input lines till sensing the trigger condition.

All other logic analyzers use infinitely-flexible pattern-matching electronics that eat up a lot of logic.

The Ganssle Group, www.ganssle.com

Mr. Wilson does correctly identify the problems with dynamically reprogramable FPGAs. First, we're talking about a whole new paradigm for design, one that requires a different mindset. Second, and more difficult, is that the tools just aren't there yet. In essence, dynamically reprogramming an ASIC means doing the routing in your system more or less in real time. Canned packages from the chip vendors would go a long way to making their products useful in these arenas where ASICs simply cannot compete.

We users need to demand better tools from the vendors. An awful lot of embedded systems could benefit. How many applications replace fixed logic with expensive DSPs, merely to achieve flexibility? Perhaps smarter use of FPGAs might reduce costs and hit even higher speeds. The opportunities are endless.

One of the PodAlyzer's designers worked for Xilinx, so knew how to route FPGAs despite the lack of tools. I've always admired his design.

Hats off to Ron Wilson for bringing up a neglected subject that has an ocean of potential.

Thought for the Week

Actual news story, 1/11/2001:

NEW YORK (Reuters) - Unisys Corp., Microsoft Corp. and Dell Computer Corp. are teaming up to create new voting technology in the wake of the ballot-counting fiasco in the U.S. presidential election, Unisys said on Thursday.

Blue Bell, Pa.-based Unisys said its system will replace outdated systems that produce irregularities such as those reported in Florida in the November election.

The system will integrate election processes from voter registration to counting results, Unisys said.

Follow-up stories:

BLUE BELL, PA (November 12, 2002) - After being unable to recover the results of last week's congressional election, the Unisys Help Desk closed the ticket today with a recommendation to reboot the system and try the election again.

REDMOND, WA (October 25, 2004) - Microsoft announced today that because of production delays in Election '04, next month's presidential election has been pushed back to the 2nd Quarter of next year.

WASHINGTON (August 3, 2005) - President George W. Bush and former Vice President Al Gore conceded today's election at 8 pm after preliminary results showed them losing overwhelmingly. Final results, released immediately after polls closed in Hawaii, showed both the incumbent Republican and his Democratic challenger failed to garner 100 votes nationwide. Former Louisiana gubernatorial candidate David Duke finished in second place with 3,322 votes on the strength of strong returns from Palm Beach County, Florida. The winning ticket received 1,073,741,824 votes -- all write-ins. "President-elect Gates and I are honored and humbled by this historic victory," said Vice President-elect Michael Dell in his acceptance speech.

About The Embedded Muse

The Embedded Muse is an occasional newsletter sent via email by Jack Ganssle. Send complaints, comments, and contributions to him at jack@ganssle.com.

To subscribe, send a message to majordomo@ganssle.com, with the words "subscribe embedded *your-email-address*" in the body. To unsubscribe, change the message to "unsubscribe embedded *your-email-address*".

The Embedded Muse is supported by The Ganssle Group, whose mission is to help embedded folks get better products to market faster. We offer seminars at your site offering hard-hitting ideas - and action - you can take now to ***improve firmware quality and decrease development time***. Contact us at info@ganssle.com for more information.